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programmable logic device (PLD) bandwidth, including, core processing, embedded memory, routing, and I/O ... standard for a **boundary-scan**-based in-system ...

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Samples are artificially generated and in no way represent ...

Did much work with **Boundary Scan** JTAG test development. ... low frequency VCO design; Altera MAX+II design tools for PLD **Programmable Logic Device** design. ...

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Terms and Definitions

A **programmable logic device** which consists of an AND array forming logical products ... A finite state machine used to control the **boundary scan** interface. ...

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EP patents matching keyword 'circuit'

EP531158, Method of and apparatus for encryption and **decryption** of communication ... EP640920, **Boundary-scan**-based system and method for test and diagnosis. ...

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EP patents matching keyword 'program'

EP607657, **Programmable logic device** and method of operation ... EP464562, Method and apparatus for **decryption** of an information packet having a format ...

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Ñiäãðæàîèä. Altera Digital Library 2002

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... Software/System Design/Distribution: BSD**L Boundary Scan** Description ...

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EP patents published 1995

EP640920, **Boundary-scan**-based system and method for test and diagnosis. ...

EP679978, Method and apparatus enabling software trial using a **decryption** stub. ...
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EP patents published 1993

EP523438, Microcomputer with **boundary-scan** facility. ... EP531158, Method of and apparatus for encryption and **decryption** of communication data. ...
 patent.tange.dk/ziki/indices/year/1993/ - 384k - [Cached](#) - [Similar pages](#)

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Boundary-Scan Description Language (software) ... Encryption-**Decryption**-Envryption
 ... High-Capacity **Programmable-Logic Device** ...

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Problem diagnosis and **boundary scan** testing is facilitated through support ...

APEX 20K **Programmable Logic Device** Family Data Sheet. ...

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... Software/System Distribution BSD**L Boundary Scan** Description Language BSF Bit

... CMOS **Programmable Logic Device** CPLD Complex **Programmable Logic Device** ...

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Dictionary Contents: all

... bounce; bounce message; **boundary scan**; boundary value analysis; bounded; ...

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... CPLD CMOS **Programmable Logic Device** CPLD Complex **Programmable Logic Device**

... Display Manager GDE Generic **Decryption** Engine GDF Geographic Data Format ...

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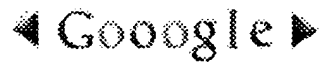
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... and other applications, such as encryption and **decryption**, and digital ... do you get it into the **programmable-logic device** or, for ... **BOUNDARY SCAN TAP CONTROLLER** ...
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... Logic Data Book, which describe device- specific information on Xilinx device characteristics, including readback, **boundary scan**, configuration, length count ...
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Ing-Jer Huang, Tai-An Lu

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C. Metra, G. Mojoli, S. Pastore, D. Salvi, G. Sechi

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This paper presents a novel technique for testing Field Programmable Gate Arrays (FPGAs), suitable to be used in case of frequent FPGA reuse and rapid dynamic modifiability of the implemented function.

Keywords: Field Programmable Gate Arrays, testing, diagnosis, reuse**4 Designing SoCs for yield improvement: Using embedded FPGAs for SoC yield improvement**

Miron Abramovici, Charles Stroud, Marty Emmert

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In this paper we show that an embedded FPGA core is an ideal host to implement infrastructure IP for yield improvement in a bus-based SoC. We present methods for testing, diagnosing, and repairing embedded FPGAs, for which complete testability is achieved without any area overhead or performance degradation. We show how an FPGA core can provide embedded testers for other cores in the SoC, so that cores designed to be tested with external vectors can be tested with BIST, and the entire SoC can be ...

5 Diagnosing programmable interconnect systems for FPGAs



Fabrizio Lombardi, David Ashen, Xiaotao Chen, Wei Kang Huang

February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**

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6 CRUSADE: hardware/software co-synthesis of dynamically reconfigurable heterogeneous real-time distributed embedded systems



Bharat P. Dave

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20-24 Sept. 1993 Page(s):410 - 415

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Patel, R.; Myron Wong; Costello, J.; Reese, D.; Bocchino, V.; Chu, M.; Turner, J.;
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995
1-4 May 1995 Page(s):507 - 510

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